(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 664 617 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **95300232.6**

(51) Int. Cl.[6] : **H03L 7/183,** H03L 7/107

(22) Date of filing : **13.01.95**

(30) Priority : **19.01.94 JP 4180/94**

(43) Date of publication of application :
26.07.95 Bulletin 95/30

(84) Designated Contracting States :
DE FR GB IT

(71) Applicant : **JAPAN RADIO CO., LTD**
1-1, Shimorenjaku 5-chome
Mitaka-shi Tokyo 181 (JP)

(72) Inventor : **Yamashita, Kazuo, c/o Japan Radio Co., Ltd.**
1-1, Shimorenjaku 5-chome
Mitaka-shi, Tokyo 181 (JP)

Inventor : **Inoue, Akiharu, c/o Japan Radio Co., Ltd.**
1-1, Shimorenjaku 5-chome
Mitaka-shi, Tokyo 181 (JP)
Inventor : **Egawa, Masahiko, c/o Japan Radio Co., Ltd.**
1-1, Shimorenjaku 5-chome
Mitaka-shi, Tokyo 181 (JP)
Inventor : **Sakuma, Hiroaki, c/o Japan Radio Co., Ltd.**
1-1, Shimorenjaku 5-chome
Mitaka-shi, Tokyo 181 (JP)
Inventor : **Adachi, Nobuyuki, c/o Japan Radio Co., Ltd.**
1-1, Shimorenjaku 5-chome
Mitaka-shi, Tokyo 181 (JP)

(74) Representative : **Cross, Rupert Edward Blount et al**
BOULT, WADE & TENNANT
27 Furnival Street
London EC4A 1PQ (GB)

(54) PLL synthesizer.

(57) The time constant determined by a high-speed time constant circuit (32) is suitable for high-speed pulling of an output frequency (f_0) , and the time constant determined by the low-speed time constant circuit (33, 34) is suitable for stabilization of the output frequency (f_0) at a corresponding value and suppression of a spurious output frequency. When the output frequency (f_0) is switched from (f_a) to (f_b), for example, the output frequency (f_0) is switched by setting the frequency division ratio (n) in the state in which the switch (S_a) is ON, while the switch (S_b) is OFF. Simultaneously, the switch (S_a) is turned off, and after the output frequency (f_0) is stabilized, the switch (S_b) is turned on. The speed of switching the output frequency (f_0) is heightened and a spurious output frequency after switching the frequency is suppressed without using an A/D converter or a D/A/ converter having high accuracy.

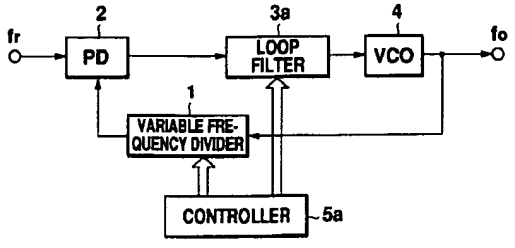

Fig. 1

EP 0 664 617 A2

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a PLL (Phase Locked Loop) synthesizer which is used for a press-to-talk wireless installation, a digital cellular telephone, a digital cordless telephone, etc., and a method of controlling such a PLL synthesizer.

Description of the Prior Art

A PLL synthesizer having a structure such as that shown in Fig. 9 is conventionally known. Fig. 9 schematically shows the structure of, for example, a "Hi-speed Digital Loop-Preset (DLP) Frequency Synthesizer", Yoshiaki TARUSAWA, and Yasushi YAMAO, NTT Radio Communication Systems Laboratories, which is described in The Reports of Technical Researches of the Institute of Electronics and Communication Engineers of Japan, 1989 Autumn B-545, pp 2-215.

In this structure, the PLL is composed of a variable frequency divider 1, a phase detector (PD) 2, a loop filter 3 and a voltage controlled oscillator (VCO) 4. The VCO 4 oscillates at an output frequency f_0 which is dependent upon the control voltage supplied from the PD 2 via the loop filter 3 and the adder 8. The VCO 4 supplies the oscillated signal to a circuit (not shown) at a subsequent stage. The output frequency f_0 produced by the VCO 4 is divided by the variable frequency divider 1 and the divided frequency is supplied to the PD 2.

It is possible to set the frequency division ratio down to a value smaller than one. If it is assumed that the frequency division ratio is n, the frequency supplied from the variable frequency divider 1 to the PD 2 is f_0/n. The PD 2 compares the frequency of the signal supplied from the variable frequency divider 1 with a reference frequency f_r which is the reference of the output frequency f_0. In other words, the PD 2 detects the phase and produces a control voltage of the VCO 4 on the basis of the result of the detection. The loop filter 3 provided at the subsequent stage to the PD 2 has a time constant which is necessary for stabilizing the output frequency f_0 of the PLL. The control voltage produced by the PD 2 is supplied to the VCO 4 via the loop filter 3. In this way, the output frequency f_0 is so controlled as to have the value n times as large as the reference frequency f_r.

In the structure shown in Fig. 9, a controller 5, an A/D converter 6, a D/A converter 7 and an adder 8 are further provided. The controller 5 digitally sets the frequency division ratio n of the variable frequency divider 1 in correspondence with the required output frequency f_0. That is, the PLL shown in Fig. 9 serves as the DLP (Digital Loop Preset). The controller 5 uses the A/D converter 6, the D/A converter and the adder 8 in order to switch the output frequency f_0.

The control voltage of the VCO 4 is first converted into a digital value by the A/D converter 6. The digital control voltage is stored in the controller 5. These processings are executed in advance with respect to various output frequencies f_0. In order to switch the output frequency f_0 to a different output frequency f_0, the controller 5 takes out the control voltage which corresponds to the necessary output frequency f_0. The D/A converter 7 converts the control voltage taken out by the controller 5 into an analog signal and supplies it to the adder 8. Simultaneously, the controller 5 resets the variable frequency divider 1.

According to the structure shown in Fig. 9, the PLL synthesizer which is capable of switching the output frequency f_0 at high speed is realized. For example, the PLL synthesizer can shorten the time required for switching the output frequency f_0 in a hands off mode or with the roaming of the zone of mobile communication, and it is suitable for a band of 1.5 GHz.

Fig. 10 schematically shows the structure of a PLL synthesizer such as "Frequency Synthesizer with Short Switching time for Digital Mobile Radio Communication", Toshimitsu KIBAYASHI, Yoshifumi TODA and Susumu SASAKI, Fujitsu Limited, which is described in The Reports of Technical Researches of the Institute of Electronics and Communication Engineers of Japan, 1990 Autumn B-308, pp 2-308. In Fig. 10, the drawing is simplified in order to clarify the difference between the prior art and the present invention.

The PLL synthesizer shown in Fig. 10 is composed of a frequency divider 9, a PD 2, a loop filter 3 and a VCO 4. The time constant of the loop filter 3 is set by using a controller 5, a ROM 10 and a D/A converter 11.

When the output frequency f_0 of the VCO 4 is switched, the controller 5 controls the read-out operation of the ROM 10 such that the data corresponding to the output frequency f_0 is output from the ROM 10. The D/A converter 11 converts the data into an analog signal and supplies the signal to the loop filter 3. The time constant of the loop filter 3 is determined by a capacitor (not shown) provided therein, and the capacitor is charged by the output of the D/A converter 11.

According to this structure, it is possible to switch the control voltage of the VCO 4 at high speed and, hence, to change the output frequency f_0 to the required output frequency f_0 at high speed. For example, it is possible to change the output frequency f_0 from 1387 MHz to 1412 MHz within 2 m sec.

As described above, various methods of enhancing the speed of switching the output frequency f_0 in a PLL synthesizer have conventionally been proposed. These methods, however, require an A/D converter and/or a D/A converter having a high accuracy, so that the circuit structure is complicated.

For example, the case of using the circuit structure shown in Fig. 9 or 10 in a local oscillator for quadrature phase shift keying (QPSK) demodulation will be considered. If the output of the reference oscillator is input as the reference frequency f_r, in order to enable digital QPSK demodulation while switching the output frequencies f_0 with a difference of about 15 MHz, it is necessary to converge (stabilize) the output frequency f_0 on the target frequency with an error of less than about 200 Hz in about 1 msec.

In order to stabilize the output frequency f_0 in about 1 m sec in the structure shown in Fig. 9, the error of the frequency output from the variable frequency divider 1 must be not more than 4 kHz, and the digital data which shows the frequency division ratio n supplied from the controller 5 to the variable frequency divider 1 is required to have an accuracy high enough to realize the stabilization. That is, in order to switch the frequencies with a difference of about 15 MHz, the A/D converter 6 and the D/A converter 7 are required to have an accuracy of not less than 12 bits.

In the structure shown in Fig. 10, in order to switch the frequencies with a difference of about 15 MHz in about 1 msec with an error of less than about 200 Hz, the D/A converter 11 is required to have accuracy of not less than 17 bits. In addition, in the structure shown in Fig. 10, since the capacitor of the loop filter 3 is charged by the output of the D/A converter 11, the charges of the capacitor are lost in the circuit at the subsequent stage before the end of the frequency changing, so that there is a limitation to high-speed frequency changing.

As a method of switching the output frequency f_0 at high speed without using the D/A converter or the A/D converter having such a high accuracy, for example, a method of using two PLLs is put to practical use. In this method, one of the PLLs is used for producing the output frequency f_0 at the present time and the other PLL prepares the output frequency f_0 for the next time. However, this method, which requires a circuit twice as large as the circuit required in the method of using only one PLL, is disadvantageous from a point of view of reduction in the size of the circuit, the cost and the power consumption.

SUMMARY OF THE INVENTION

Accordingly, it is a first object for particular embodiments of the invention to eliminate the above-described problems in the prior art and to enable high-speed switching of output frequencies without using a plurality of PLLs, thereby realizing a reduction in the size of the circuit, the cost and the power consumption.

It is a second object for particular embodiments to enable high-speed switching of output frequencies without using a D/A converter or an A/D converter having high accuracy, thereby simplifying the circuit structure.

It is a third object for particular embodiments to stabilize the output frequency at a speed which is appropriate for, for example, digital QPSK demodulation.

It is a fourth object for particular embodiments to suppress a spurious output frequency produced after switching the frequencies due to an error of the reference frequency of the PLL or the slip frequency generated due to division with a ratio down to a value smaller than one.

To achieve these objects, in a first aspect of the present invention, there is provided a PLL synthesizer comprising: an oscillator for oscillating at an output frequency which depends upon a control voltage supplied thereto; a frequency divider for dividing the output frequency in correspondence with a required output frequency; a detector for detecting a phase of a frequency-divided output frequency by referring to a reference frequency which is the reference of the output frequency so as to produce the control voltage; and a loop filter for stabilizing the output frequency by filtering the control voltage produced by the detector and supplying a filtered control voltage to the oscillator; the loop filter including;

a) a high-speed time constant circuit constantly inserted between the detector and the oscillator and having a predetermined first time constant so set that when the required output frequency is changed, the output frequency produced by the oscillator is stepwisely changed to a new output frequency at high speed;

(b) a low-speed time constant circuit which is inserted between the detector and the oscillator as occasion demands and which has a predetermined second time constant so set that a spurious output frequency produced due to an error of the reference frequency or an error of the frequency-divided output frequency is suppressed when the low-speed time constant circuit is inserted between the detector and the oscillator; and

(c) switching means for making and breaking a signal path between the detector and the oscillator via the low-speed time constant circuit as occasion demands.

In a PLL synthesizer provided in a second aspect of the present invention, the PLL synthesizer of the first aspect is further provided with a plurality of output frequencies are prepared, the plurality of output frequencies including at least first and second frequencies; and a plurality of pairs of low-speed time constant circuits and switching means are arranged in parallel, each of which is provided with in correspondence with one of the plurality of output frequencies. The PLL synthesizer further comprises a controller for controlling the frequency divider and the switching means in accordance with a predetermined

processing;

the controller including:

a) means for switching the output frequency from the first frequency to the second frequency by controlling the frequency divider;

b) means for breaking the signal path between the detector and the oscillator via the low-speed time constant circuit which corresponds to the first frequency by controlling the switching means which corresponds to the first frequency when the output frequency is to be switched from the first frequency to the second frequency; and

c) means for making the signal path between the detector and the oscillator via the low-speed time constant circuit which corresponds to the second frequency by controlling the switching means which corresponds to the second frequency after the output frequency is changed in a stepwise manner to the second frequency.

In a third aspect of the present invention, there is provided a PLL synthesizer similar to that provided in the first aspect and further comprising a controller for controlling the frequency divider and the switching means in accordance with predetermined processing, the controller including:

a) means for switching a frequency division ratio of the frequency divider to the value which corresponds to a temporary frequency when the output frequency is to be temporarily switched from a communication frequency to the temporary frequency;

b) means for switching the time constant of the loop filter to a value smaller than a usual value by controlling the switching means when the output frequency is to be temporarily switched from the communication frequency to the temporary frequency;

c) means for switching the frequency division ratio of the frequency divider to a value which corresponds to the communication frequency when the output frequency is to be returned to the communication frequency; and

d) means for switching the time constant of the loop filter to a value which corresponds to the communication frequency and which is suitable for suppressing a spurious output frequency by controlling the switching means after the output frequency is returned to the communication frequency.

In the PLL synthesizers provided in the first to third aspects of the present invention, it is possible to switch the time constant of the loop filter between a time constant which is comparatively small and a time constant which is comparatively large. More specifically, when only the high-speed time constant circuit is inserted between the detector and the oscillator, the time constant of the loop filter becomes a comparatively small time constant which is determined only by that of the high-speed time constant circuit. In this state, if the frequency division ratio of the frequency divider is set in correspondence with the required output frequency so as to switch the output frequency of the oscillator, the output frequency of the oscillator is changed in a stepwise manner to a new frequency at high speed. On the other hand, when the low-speed time constant circuit is inserted between the detector and the oscillator by the operation of the switching means, the time constant of the loop filter becomes a comparatively large time constant which is mainly determined by the low-speed time constant circuit. In this state, the time constant of the loop filter is too large to change the output frequency at high speed. However, by utilizing the low-speed time constant circuit, it is possible to suppress a spurious output frequency produced due to an error of the reference frequency which is supplied to the detector or an error of the frequency division of the frequency divider (e.g., slip frequency due to the division by a ratio with a value smaller than one).

For example, when a PLL synthesizer is used for a local oscillator of a wireless installation (e.g., press-to-talk wireless installation, stations of a digital mobile telephone system and those of a digital cordless telephone system) in which the transmitted frequency is different from the received frequency, to use the installation, there is a method of A) switching the output frequencies of the PLL synthesizer between the frequencies which correspond to the transmitted frequency and the received frequency, and B) a method of dealing with the difference between the transmitted frequency and the received frequency using external equipment without switching the output frequency throughout the transmission and reception.

In the case of adopting the method A), the PLL synthesizer provided in any of the first to third aspects of the present invention can be utilized for high-speed frequency changing or the suppression of a spurious output frequency at the time of switching between the transmitted frequency and the received frequency.

According to the PLL synthesizer provided in the second aspect of the present invention, at the time of switching the output frequency of the oscillator (e.g., VCO) constituting the PLL synthesizer from the first frequency to the second frequency, the frequency division ratio of the frequency divider is changed from the value which corresponds to the first frequency to the value which corresponds to the second frequency, and the signal path via the low-speed time constant circuit which corresponds to the first frequency is broken by the control of the switching means. By this operation, the time constant of the loop filter becomes a value which is suitable for high-speed frequency changing, thereby changing the frequency to the second frequency at high speed.

In addition, according to the PLL synthesizer provided in the second aspect of the present invention,

after the output frequency is changed to the second frequency, the controller produces a signal path via the low-speed time constant circuit which corresponds to the second frequency. When the low-speed time constant circuit is inserted between the detector and the oscillator, it suppresses the production of a spurious output frequency due to an error of the reference frequency and/or an error of the frequency division of the frequency divider. Therefore, the production of a spurious output frequency, after the end of frequency changing, is suppressed. The number of the low-speed time constant circuits is not restricted to two.

Even if the method B) of not switching the output frequency through the transmission and reception is adopted when using the PLL synthesizer, the PLL synthesizer provided in the third aspect of the present invention is useful. For example, in a system adopting a TDMA (Time Division Multiple Access) system represented by a a mobile telephone system such as PDC in Japan and TIA in USA and a digital cordless telephone system such as PHS (Personal Handiphone System) in Japan, while signals are transmitted or received by using a predetermined frequency channel, the carrier sensing is carries out at a predetermined time (in a time slot in which neither transmission nor reception is conducted) so as to judge whether or not a signal at a significant level exists in other frequency channels. In the PLL synthesizer used for such applications, the output frequency of the PLL synthesizer used as the local oscillator is not switched at the time of switching from transmission to reception and vice versa, but it is switched when the operation is shifted from the transmission or the reception to the carrier sensing. Particular embodiments of the present invention are applicable to this switching. Adoption of these embodiments heightens the speed of changing the frequency to the frequency which is to be the object of monitoring and suppresses a spurious output frequency which may be produced when the frequency is returned to the transmitted or received frequency. In the PLL synthesizer used for this purpose, since the frequency which is to be the object of monitoring is not used for communication, there is no problem of producing a spurious output frequency at this frequency. Accordingly, one low-speed time constant circuit suffices.

As described above, according to particular embodiments of the invention, it is possible to produce a PLL synthesizer which is suitable for monitoring other frequency channels or switching of the output frequency without the need for an A/D converter and/or a D/A converter having a high accuracy. It is possible to heighten the speed of frequency switching by using a high-speed time constant circuit and suppressing a spurious output frequency after switching the frequency by using a low-speed time constant circuit. For example, even if the output frequencies are switched with a difference of about 15 MHz, it is possible to stabilize the output frequency f_0 with an error of less than about 200 Hz in about 1 msec, thereby favorably enabling digital QPSK demodulation. In addition, the production of a spurious output frequency due to the error of the reference frequency supplied to the PLL or the slip frequency due to the division to a ratio with a value smaller than one is favorably suppressed. As a result, it is possible to produce a PLL synthesizer which is suitable for a press-to-talk wireless installation, a digital cellular telephone, a digital cordless telephone, etc., and which has a small size at a low cost.

The low-speed time constant circuit may be composed of a resistor and a capacitor connected in series. In the low-speed time constant circuit having this structure, a spurious output frequency is suppressed by the charges stored in the capacitor. Since the capacitor is kept changed by breaking the signal path via the low-speed time constant circuit, the voltage of the capacitor is held by until the signal path via the low-speed time constant circuit is completed later. Therefore, the high-frequency component of the output of the detector which causes a spurious output frequency is absorbed by the capacitor without producing a fluctuation in the output frequency. When a plurality of low-speed time constant circuits are prepared, at least one part of the resistors which constitute respective low-speed time constant circuits may be shared by other low-speed time constant circuits. In this manner, the structure of the apparatus may be simplified.

In a fourth aspect of the present invention, there is provided a controlling apparatus comprising:

a) means for switching a frequency division ratio of a frequency divider to a value which corresponds to a second frequency when an output frequency is to be switched from a first frequency to the second frequency;

b) means for switching a time constant of a loop filter from a value which corresponds to the first frequency and which is suitable for suppressing a spurious output frequency to a value which is suitable for high-speed frequency changing when the output frequency is to be switched from the first frequency to the second frequency; and

c) means for switching the time constant of the loop filter from the value which is suitable for the high-speed frequency changing to a value which corresponds to the second frequency and which is suitable for suppressing the spurious output frequency.

In a fifth aspect of the present invention, there is provided a controlling apparatus comprising:

a) means for switching a frequency division ratio of a frequency divider to a value which corresponds to a temporary frequency when an output frequency is to be switched from a communica-

tion frequency to the temporary frequency;

b) means for switching a time constant of a loop filter to a value smaller than a usual value when the output frequency is to be switched from the communication frequency to the temporary frequency;

c) means for switching the frequency division ratio of the frequency divider to a value which corresponds to the communication frequency when the output frequency is returned to the communication frequency; and

d) means for switching the time constant of the loop filter to the value which corresponds to the communication frequency and which is suitable for suppressing a spurious output frequency after the output frequency is returned to the communication frequency.

In a sixth aspect of the present invention, there is provided a controlling method comprising the steps of:

a) switching a frequency division ratio of a frequency divider to a value which corresponds to a second frequency when an output frequency is to be switched from a first frequency to the second frequency;

b) switching a time constant of a loop filter from a value which corresponds to the first frequency and which is suitable for suppressing a spurious output frequency to a value which is suitable for high-speed frequency changing when the output frequency is to be switched from the first frequency to the second frequency; and

c) switching the time constant of the loop filter from the value which is suitable for the high-speed frequency changing to a value which corresponds to the second frequency and which is suitable for suppressing the spurious output frequency after the output frequency is changed to the second frequency.

In a seventh aspect of the present invention, there is provided a controlling method comprising the steps of:

a) switching a frequency division ratio of a frequency divider to a value which corresponds to a temporary frequency when an output frequency is switched from a communication frequency to the temporary frequency;

b) switching a time constant of a loop filter to a value smaller than a usual value when the output frequency is to be switched from the communication frequency to the temporary frequency;

c) switching a frequency division ratio of the frequency divider to a value which corresponds to the communication frequency when the output frequency is to be returned to the communication frequency; and

d) switching the time constant of the loop filter to a value which corresponds to the communication frequency and which is suitable for suppressing a spurious output frequency after the output frequency is returned to the communication frequency.

The controlling apparatus and the controlling method provided in the fourth and sixth aspects of the present invention are suitable for embodying the second aspect of the present invention, and the controlling apparatus and the controlling method provided in the fifth and seventh aspects of the present invention are suitable for embodying the third aspect of the present invention.

The above and other objects, features and advantages of the present invention will become clear from the following description of the preferred embodiments thereof, taken in conjunction with the accompanying single drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram schematically showing the structure of first and second embodiments of a PLL synthesizer according to the present invention;

Fig. 2 is a circuit diagram showing the structure of the main part, particularly, the inner part of the loop filter of the first embodiment of the present invention;

Fig. 3 is a timing chart showing the frequency stabilizing speed when a frequency is switched while the switch Sa is held ON;

Fig. 4 is a timing chart showing the frequency stabilizing speed when a frequency is switched while controlling the switches Sa and Sb;

Fig. 5 is a flow chart of the controlling process when the frequency is switched from f_a to f_b;

Fig. 6 is a flow chart of the controlling process when the frequency is switched from f_b to f_a;

Fig. 7 is a flow chart of the controlling process when the frequency is monitored;

Fig. 8 is a circuit diagram showing the structure of the main part, particularly, the inner part of the loop filter of the second embodiment of the present invention;

Fig. 9 is a block diagram schematically showing the structure of a conventional PLL synthesizer; and

Fig. 10 is a block diagram schematically showing the structure of another conventional PLL synthesizer.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the present invention will now be explained in more detail with reference to the accompanying drawings. The same reference numerals are provided for the elements which

are the same as those in the prior art shown in Fig. 9 and 10, and explanation thereof will be omitted.

a) Overall structure of a first embodiment

Fig. 1 schematically shows the structure of a first embodiment of a PLL synthesizer according to the present invention. In this structure, the PLL is composed of a variable frequency divider 1, a PD 2, a loop filter 3a and a VCO 4. A controller 5a digitally controls the frequency division ratio of the variable frequency divider 1 down to a value smaller than one. That is, the PLL synthesizer shown in Fig. 1 serves as a kind of DLP synthesizer. The controller 5a enables the switching of the output frequency f_0 at high speed and favorably suppresses a spurious output frequency by switching the switch provided in the loop filter 3a.

b) Structure of the loop filter 3a in the first embodiment

Fig. 2 shows the structure of the loop filter 3a in this embodiment. The loop filter 3a is composed of an operational amplifier 31, a high-speed time constant circuit 32, and low-speed time constant circuits 33, 34.

The high-speed time constant circuit 32 is composed of resistors R, R_h, and capacitors C_{hs}, C_h. The resistor R is provided between the input terminal of the loop filter 3a and the inverting input terminal of the operational amplifier 31. Both one end of the resistor R_h and one end of the capacitor C_{hs} are connected to the inverting input terminal of the operational amplifier 31, and the resistor R_h and the capacitor C_{hs} are connected in parallel. The parallel circuit of the resistor R_h and the capacitor C_{hs} is connected to the output terminal of the operational amplifier 31 through the capacitor c_h, namely, the output terminal of the loop filter 3a. In other words, the resistor R_h and the capacitors C_{hs}, C_h constitute the feedback circuit of the operational amplifier 31. The high-speed time constant circuit 32 constituted by the feedback circuit and the input resistor R together with the operational amplifier 31 constitutes one loop filter. The time constant of the loop filter is determined by the time constant of the high-speed time constant circuit 32. In this embodiment, the time constant of the high-speed time constant circuit 32 is set at a small value which is suitable for high-speed pulling at the time of switching the output frequency f_0.

The low-speed time constant circuit 33 is composed of the resistor R, a resistor R_a, capacitors C_{as} and C_a. The resistor R_a and the capacitor C_{as} are connected in parallel with each one end connected to the inverting input terminal of the operational amplifier 31 and each of the other ends is connected to the output terminal of the operational amplifier 31 via the capacitor C_a and a switch S_a. While the switch S_a is closed and a switch S_b is opened, the low-speed time constant circuit 33 and the operational amplifier 31, together with the high-speed time constant circuit 32, constitute one loop filter. The time constant of the loop filter is mainly determined by the time constant of the low-speed time constant circuit 33. In this embodiment, the time constant of the low-speed time constant circuit 33 is set at a value which is capable of stabilizing the output frequency f_0 by a frequency f_a and suppressing a spurious output frequency.

The low-speed time constant circuit 34 is composed of the resistor R, a resistor R_b, capacitors C_{bs} and C_b. The resistor R_b and the capacitor C_{bs} are connected in parallel with each one end connected to the inverting input terminal of the operational amplifier 31 and each the other ends connected to the output terminal of the operational amplifier 31 via the capacitor C_b and the switch S_b. While the switch S_b is closed and the switch S_a is opened, the low-speed time constant circuit 34 and the operational amplifier 31 together with the high-speed time constant circuit 32 constitute one loop filter. The time constant of the loop filter is determined by the time constant of the low-speed time constant circuit 33. In this embodiment, the time constant of the low-speed time constant circuit 34 is set at a value which is capable of stabilizing the output frequency f_0 by a frequency f_b and favorably suppressing a spurious output frequency.

The controller 5a controls the switches S_a, S_b which constitute the loop filter 3a. The first embodiment is characterized by the structure of the loop filter 3a and the control process of the controller 5a.

c) Comparative example

In order to clarify the advantages of particular embodiments of the present invention and the system for bringing about the advantages, a conventional control process is shown in Fig. 3 as a comparative example. Fig. 3 shows the frequency stabilizing operation when the output frequency is switched from f_0 to f_a by controlling the frequency division ratio n of the variable frequency divider 1 while holding the switch S_a ON. In Fig. 3, it is assumed that f_a = 815 MHz and f_b = 800 MHz, and that the frequency division ratio n which is necessary for controlling the output frequency f_0 to f_a is 2037.5, and the frequency division ratio n which is necessary for controlling the output frequency f_0 to f_b is 2000.0.

As shown in Fig. 3, when the controller 5a changes the frequency division ratio n from 2037.7 to 2000.0 (time = 0) while holding the switch S_a ON, a long time is required for the output frequency f_0 to be switched from f_a to f_b. To state this concretely, the time required for stabilizing the output frequency f_0 to the frequency f_b with an error of less than about 200 Hz is more than 8 msec. If such a long time is required for switching the output frequency f_0, a PLL synthes-

izer which is suitable for a local oscillator for digital QPSK demodulation is not realized, so that favorable demodulation is impossible.

d) Process of switching a frequency

In this embodiment, the controller 5a exerts the control shown in Figs. 4 to 6 when the output frequency f_0 is switched from f_a to f_b or vice versa. Fig. 4 shows the frequency stabilizing state at the time of switching a frequency, Fig. 5 shows the controlling process of the controller 5a when the frequency is switched from f_a to f_b, and Fig. 6 shows the controlling process of the controller 5a when the frequency is switched from f_b to f_a. In these drawings, it is also assumed that f_a = 815 MHz and f_b = 800 MHz, and that the frequency division ratio n which is necessary for controlling the output frequency f_0 to f_a is 2037.5, and the frequency division ratio n which is necessary for controlling the output frequency f_0 to f_b is 2000.0.

The case of switching the output frequency f_0 from f_a to f_b (time = o) will first be considered. It is assumed that the output frequency f_0 has been controlled to the frequency f_b at a previous point in time. Due to this history, the charges necessary for stabilizing the output frequency f_0 at f_b are already stored in the capacitor C_b of the low-speed time constant circuit 34. It is also assumed that the switch S_a is ON and the switch S_b is OFF immediately before switching f_a to f_b.

When the controller 5a switches the output frequency f_0 from f_a to f_b, it first switches the frequency division ratio n of the variable frequency divider 1 from 2037.5, which corresponds to f_a, to 2000.0. which corresponds to f_b (step 100 in Fig. 5). At the same time, the controller 5a turns off the switch S_a of the loop filter 3a (step 100). Since both the switches S_a and S_b are OFF, the time constant of the loop filter 3a becomes the time constant determined by the high-speed time constant circuit 32. With this time constant, the output frequency f_0 is changed at high speed. More specifically, switching of the frequency is completed in about 0.6 msec.

Immediately after the switching of the frequency, since the time constant is the value determined by the high-speed time constant circuit 32, a slight spurious output frequency is produced, as shown in Fig. 4. In order to suppress the spurious output frequency quickly in this embodiment, the controller 5a is turned on (step 104) at a predetermined point of time after the end of switching, namely, when the output frequency f_0 is sufficiently stabilized at the frequency f_b (step 102). The time constant of the loop filter 3a then becomes a time constant determined mainly by the low-speed time constant circuit 34. This is because the capacitor C_b which constitutes the low-speed time constant circuit 34 has a large capacitance than the capacitor C_h.

Consequently, by turning on the switch S_b with the timing shown in Fig. 4, the noise of the reference frequency f_r or the slip frequency caused by the divider 1 and, hence, the spurious output frequency are suppressed. The charges necessary for stabilizing the output frequency f_0 at f_b are already stored in the capacitor C_b while the switch S_b is ON. As a result, when the output frequency f_0 has been controlled to be the frequency f_b at a preceding point in time, as described above, by turning on the switch S_b with the timing shown in Fig. 4, the above-described advantages are produced without fluctuation of the output frequency f_0.

When the output frequency f_0 is switched from the frequency f_b to the frequency f_a (the right half in Fig. 4, and Fig. 6), the switch S_b is turned off (step 106) in the state in which the switch S_b is ON, and after the output frequency f_0 is changed to the frequency f_a (step 108), the switch S_a is turned on (step 110).

In this embodiment, the output frequency f_0 is switched between f_a and f_b, but the number of output frequencies is not restricted to two. In the case of providing three different output frequencies for f_0, the number of low-speed time constant circuits provided is changed to three. Such modification will be easy to those skilled in the art by reference to the specification and the drawings of the present application.

This embodiment of the PLL synthesizer is used for a local oscillator for switching the local oscillation frequency (output frequency f_0 of the PLL synthesizer). Such an operation of switching the local oscillation frequency may be adopted not only when the the transmitted frequency or the received frequency is switched to a frequency in another channel but also when the transmitted frequency is switched to the received frequency or vice versa in a press-to-talk wireless installation.

It is because the reference frequency f_r is assumed to be 400 kHz that the frequency division ratio n of the variable frequency divider 1 is switched between 2037.5 and 2000.0 in this embodiment (815 MHz/400 kHz = 2037.5, 800 MHz/400 kHz = 2000.0). However, the reference frequency f_r may be set at any value, so that the frequency division ratio n of the variable frequency divider 1 may be set at any value.

e) Process of monitoring a frequency

The present invention is not restricted to switching of a frequency. For example, the present invention is also applicable to monitoring of a frequency executed in a wireless installation for TDMA (Time Division Multiple Access) such as a digital portable phone. The monitoring of a frequency involves the processing of temporarily receiving another frequency during the communication at a certain frequency, for example, at the frequency f_b so as to judge whether or not a carrier of the frequency exists. Fig. 7 shows the control process of the controller 5a for executing

the monitoring.

As shown in Fig. 7, the controller 5a first switches the frequency division ratio n of the variable frequency divider 1 to the value which corresponds to the frequency as the object of monitoring (step 112). At the same time, the controller 5a turns off the switch (e.g. S_b) which corresponds to the frequency at which communication has been established, thereby changing the time constant of the loop filter 3a to a comparatively small time constant which is determined by the high-speed time constant circuit 32 (step 112). After the detection of a carrier is finished by a circuit (not shown) at the subsequent stage, in other words, a predetermined monitoring period ends (step 114), the controller 5a switches the frequency division ratio n to the value (e.g., 2037.5) which corresponds to the original frequency (step 116). At the point of time where the time required for stabilization of the output frequency f_0 has elapsed (step 118), the controller 5a turns on the switch (e.g., S_b) which corresponds to the original frequency (step 120).

In this manner, it is possible to change the frequency to the frequency which is to be the object of monitoring at high speed. Since this frequency is used only for detection of a carrier and is not used for communication, the stabilization of the frequency with high accuracy, which is required in the communication of information such as voice, is not necessary. It is therefore not necessary to provide a low-speed time constant circuit for stabilizing the output frequency f_0 which is the object of monitoring.

At the time of commencing communication after the end of the detection of a carrier, the frequency is stabilized in a short time by high-frequency changing and thereafter the low-speed time constant circuit is energized so as to suppress a spurious output frequency. This operation enables high-speed changing for the purpose of communication and favorable suppression of a spurious output frequency.

f) Structure of the loop filter 3b in a second embodiment

Fig. 8 shows the structure of the main part of a second embodiment of a PLL synthesizer of the present invention. In Fig. 8, a loop filter 3b is used in place of the loop filter 3a shown in Fig. 1. The loop filter 3b is different from the loop filter 3a in that it is a lag lead type. When the control shown in Fig. 4 is exerted by the second embodiment having this structure, the effects of high-speed output frequency f_0 changing and the suppression of a spurious output frequency are brought about in the same way as by the first embodiment.

g) Advantages of the embodiments

As explained above, in each of the embodiments, the high-speed time constant circuit 32 and the low-speed time constant circuits 33, 34 are provided in the loop filter 3a or 3b, and the low-speed time constant circuits 33 and 34 are appropriately inserted in a circuit by using the switches Sa and Sb. Therefore, the PLL synthesizer which is suitable for monitoring a frequency and switching of the output frequency f_0 is obtained by using an A/D converter or a D/A converter having high accuracy. It is possible to increase the speed of switching or a frequency by using the high-speed time constant circuit 32 and to favorably suppress a spurious output frequency by using the low-speed time constant circuits 33 and 34 after switching of the output frequency f_0. For example, even if the output frequency f_0 is switched with a difference of about 15 MHz, it is possible to stabilize the output frequency f_0 with an error of less than about 200 Hz in about 1 m sec, thereby enabling digital QPSK demodulation. A spurious output frequency produced due to an error of the reference frequency f_r which is supplied to the detector or the slip frequency caused by the division using the ratio n down to a value smaller than one. As a result, it is possible to produce a PLL synthesizer which is suitable for a press-to-talk wireless installation, a digital cellular telephone, a digital cordless telephone, etc., and which has a small size at a low cost.

In each of these embodiments, the resistor R is shared by the high-speed time constant circuit 32 and the low-speed time constant circuits 33 and 34. This comparatively simplifies the structure of the apparatus.

While there has been described what are at present considered to be preferred embodiments of the invention, it will be understood that various modifications may be made thereto, and it is intended that the appended claims cover all such modifications as fall within the true spirit and scope of the invention.

Claims

1. A phase locked loop synthesizer comprising:

an oscillator (4) for oscillating at an output frequency which depends upon a control voltage supplied thereto;

a frequency divider (1) for dividing the output frequency in correspondence with a required output frequency;

a detector (2) for detecting a phase of a frequency-divided output frequency by referring to a reference frequency which is the reference of the output frequency so as to produce the control voltage; and

a loop filter (3a, 3b) for stabilizing the output frequency by filtering the control voltage produced by said detector (2) and supplying a filtered control voltage to said oscillator (4);

said loop filter (3a, 3b) including;

a high-speed time constant circuit (32) constantly inserted between said detector (2) and said oscillator (4) and having a predetermined first time constant so set that when the required output frequency is changed, the output frequency produced by said oscillator is stepwisely changed to a new output frequency at high speed;

a low-speed time constant circuit (33, 34) which is inserted between said detector (2) and said oscillator (4) as occasion demands and which has a predetermined second time constant so set that a spurious output frequency produced due to an error of the reference frequency or an error of the frequency-divided output frequency is suppressed when the low-speed time constant circuit (33, 34) is inserted between said detector and said oscillator; and

switching means for making and breaking a signal path between said detector (2) and said oscillator (4) via said low-speed time constant circuit (33, 34) as occasion demands.

2. A synthesizer according to claim 1, wherein a plurality of output frequencies (f_a, f_b) are provided, said plurality of output frequencies including at least a first frequency (e.g., fa) and a second frequency (e.g., f_b); and

a plurality of pairs of low-speed time constant circuits (33, 34) and switching means (S_a, S_b) are arranged in parallel, each of which is provided with in correspondence with one of the plurality of output frequencies;

said synthesizer further comprising a controller (5a) for controlling the frequency divider (1) and said switching means (S_a, S_b) in accordance with a predetermined processing;

said controller (5a) including:

means 100 for switching the output frequency (f_0) from the first frequency (e.g., f_a) to the second frequency (e.g., f_b) by controlling said frequency divider (1);

means 100 for breaking the signal path between the said detector (2) and said oscillator (4) via said low-speed time constant circuit (33) which corresponds to the first frequency (e.g., f_a) by controlling said switching means (e.g., S_a) which corresponds to the first frequency (e.g., f_a) when the output frequency (f_0) is to be switched from the first frequency (e.g., f_a) to the second frequency (e.g., f_b); and

means (102, 104) for making the signal path between said detector (2) and said oscillator (4) via said low-speed time constant circuit (34) which corresponds to the second frequency (e.g., f_b) by controlling said switching means (e.g., S_b) which corresponds to the second frequency (e.g., f_b) after the output frequency (f_0) is changed in a stepwise manner to the second frequency (e.g., f_b).

3. A synthesizer according to claim 1, further comprising a controller (5a) for controlling said frequency divider (1) and said switching means (S_a, S_b) in accordance with predetermined processing, said controller (5a) including:

means 112 for switching a frequency division ratio of said frequency divider (1) to the value which corresponds to a temporary frequency (e.g., f_a) when the output frequency f_0 is to be temporarily switched from a communication frequency (e.g., f_b) to the temporary frequency (e.g., f_a);

means 112 for switching the time constant of said loop filter (3a, 3b) to a value smaller than a usual value by controlling said switching means (e.g., S_b) when the output frequency (f_0) is to be temporarily switched from the communication frequency (e.g., f_b) to the temporary frequency (e.g., f_a);

means 116 for switching the frequency division ratio (n) of said frequency divider (1) to a value which corresponds to the communication frequency (e.g., f_b) when the output frequency (f_0) is to be returned to the communication frequency (e.g., f_b); and

means 120 for switching the time constant of said loop filter (3a, 3b) to a value which corresponds to the communication frequency (e.g., f_b) and which is suitable for suppressing a spurious output frequency by controlling said switching means (e.g., S_b) after the output frequency (f_0) is returned to the communication frequency (e.g., f_b).

4. A synthesizer according to claim 1, wherein

a plurality of output frequencies (f_a, f_b) are prepared;

a plurality of pairs of low-speed time constant circuits (33, 34) and switching means (S_a, S_b) are arranged in parallel, each of which is provided in correspondence with said plurality of output frequencies (f_a, f_b), each of said low-speed time constant circuits (33, 34) including a resistor (R, R_a, R_b) and a capacitor (C_a, C_{as}, C_b, C_{bs}) connected in series; and

at least one resistor (R, R_a, R_b) which constitutes one of the low-speed time constant circuits (33, 34) is shared by other ones of the low-speed time constant circuits (34, 33).

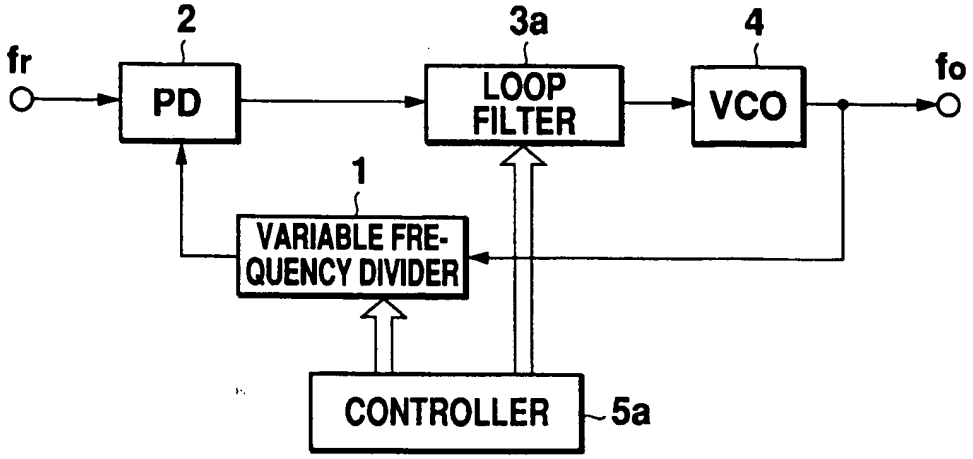
2
3a
4
fr
PD
LOOP FILTER
VCO
fo
1
VARIABLE FREQUENCY DIVIDER
CONTROLLER
5a

Fig. 1

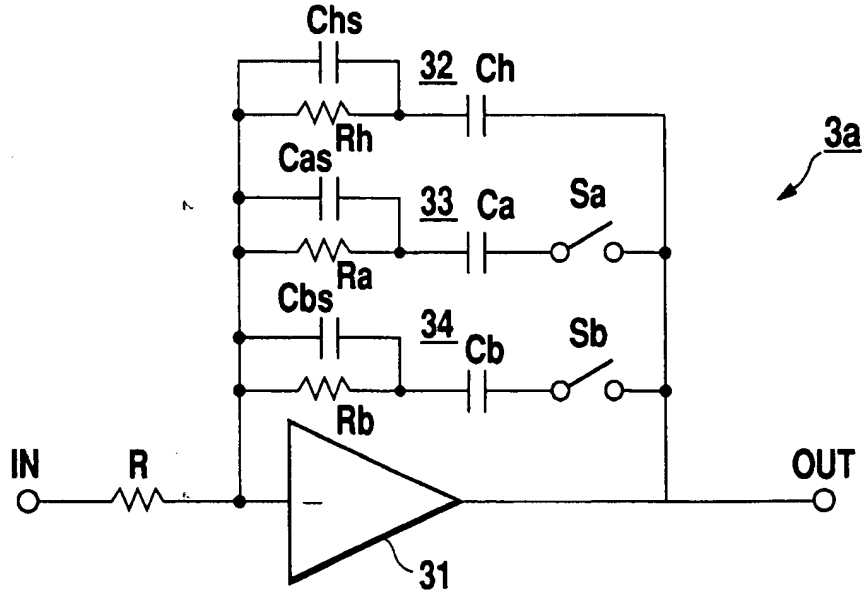
Chs
32
Ch
Rh
Cas
33
Ca
Sa
Ra
Cbs
34
Cb
Sb
Rb
3a
IN
R
OUT
31

Fig. 2

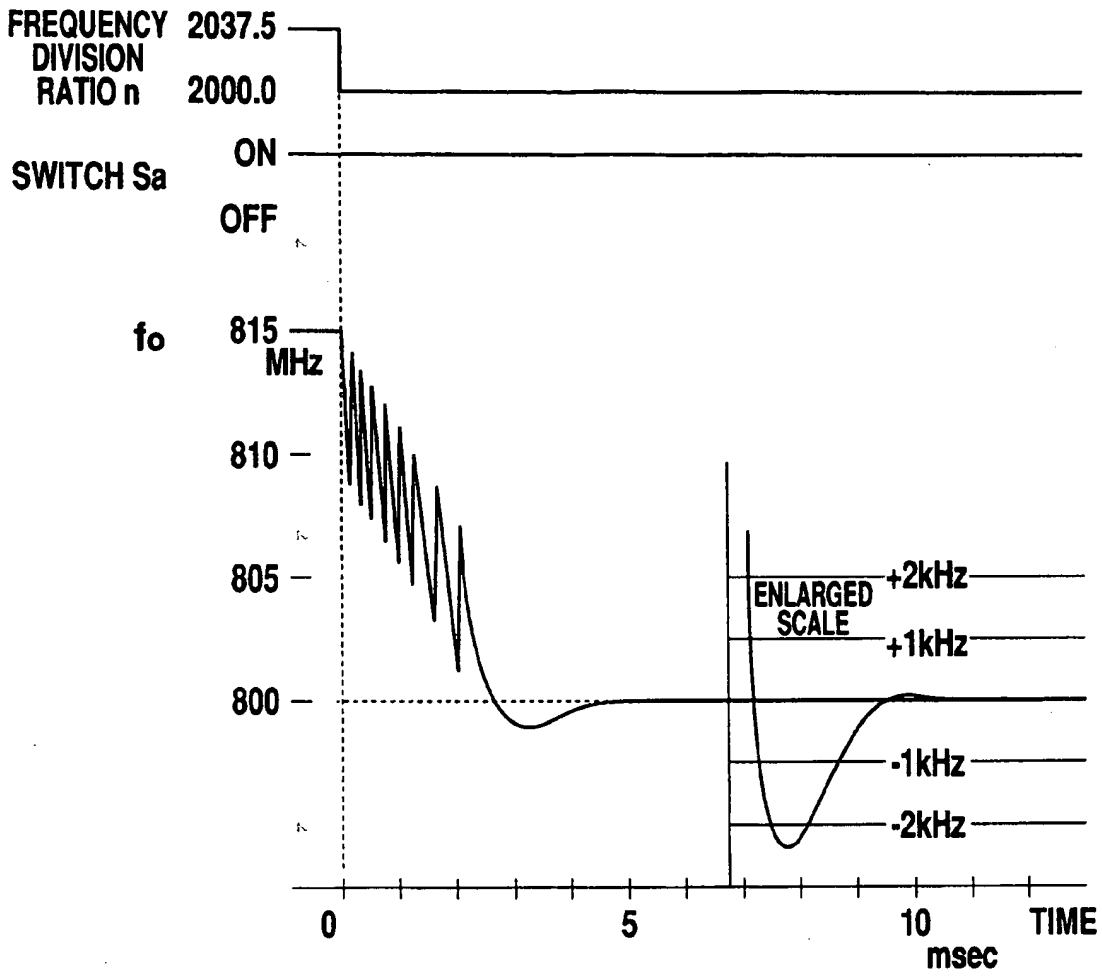
FREQUENCY DIVISION RATIO n
2037.5
2000.0
SWITCH Sa
ON
OFF
fo
815
MHz
810
805
800
ENLARGED SCALE
+2kHz
+1kHz
-1kHz
-2kHz
0
5
10
TIME
msec

Fig. 3

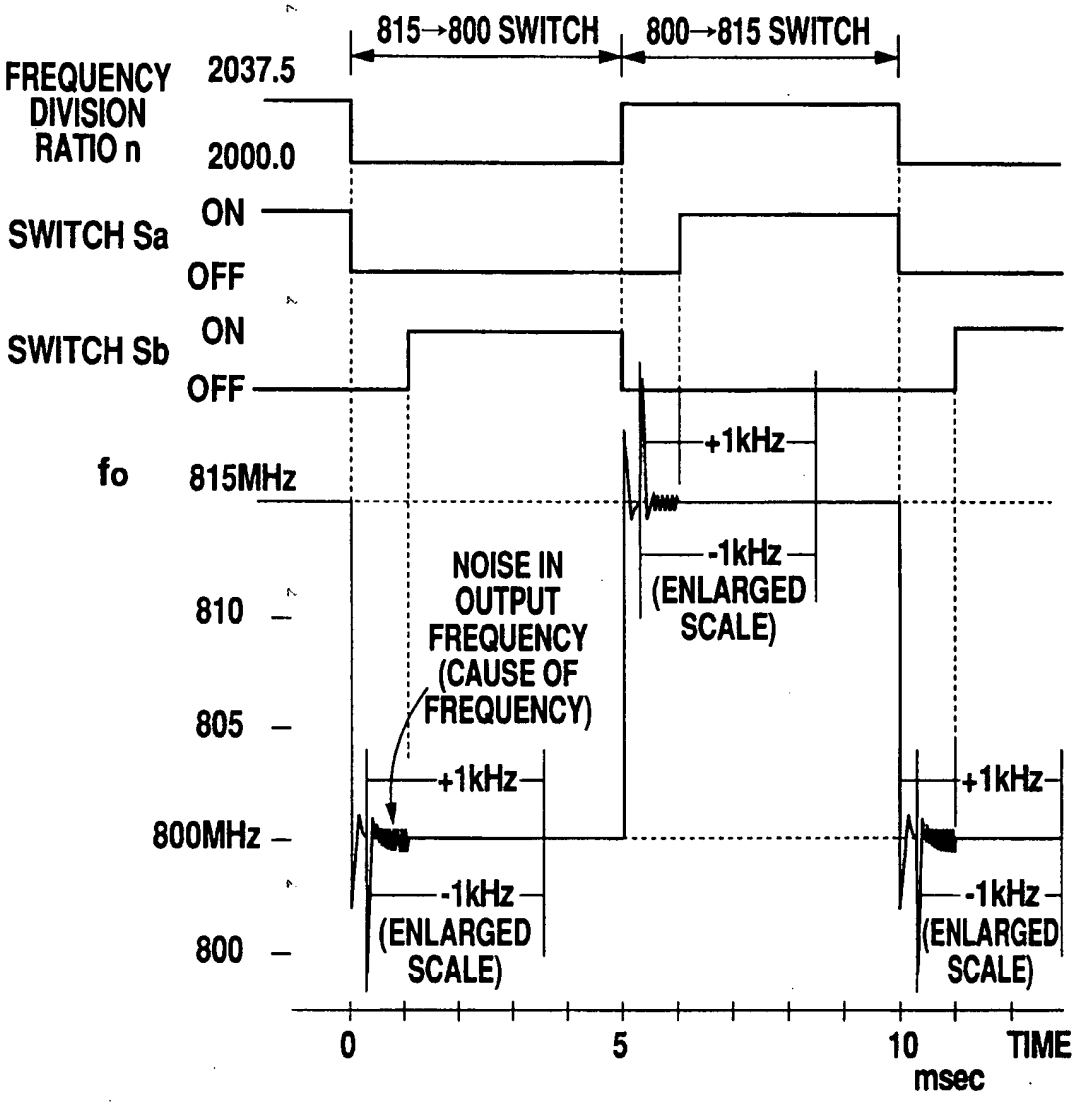
815→800 SWITCH
800→815 SWITCH
FREQUENCY DIVISION RATIO n
2037.5
2000.0
SWITCH Sa
ON
OFF
SWITCH Sb
ON
OFF
fo
815MHz
+1kHz
-1kHz
(ENLARGED SCALE)
NOISE IN OUTPUT FREQUENCY (CAUSE OF FREQUENCY)
810
805
800MHz
800
+1kHz
-1kHz
(ENLARGED SCALE)
+1kHz
-1kHz
(ENLARGED SCALE)
0
5
10
TIME
msec

Fig. 4

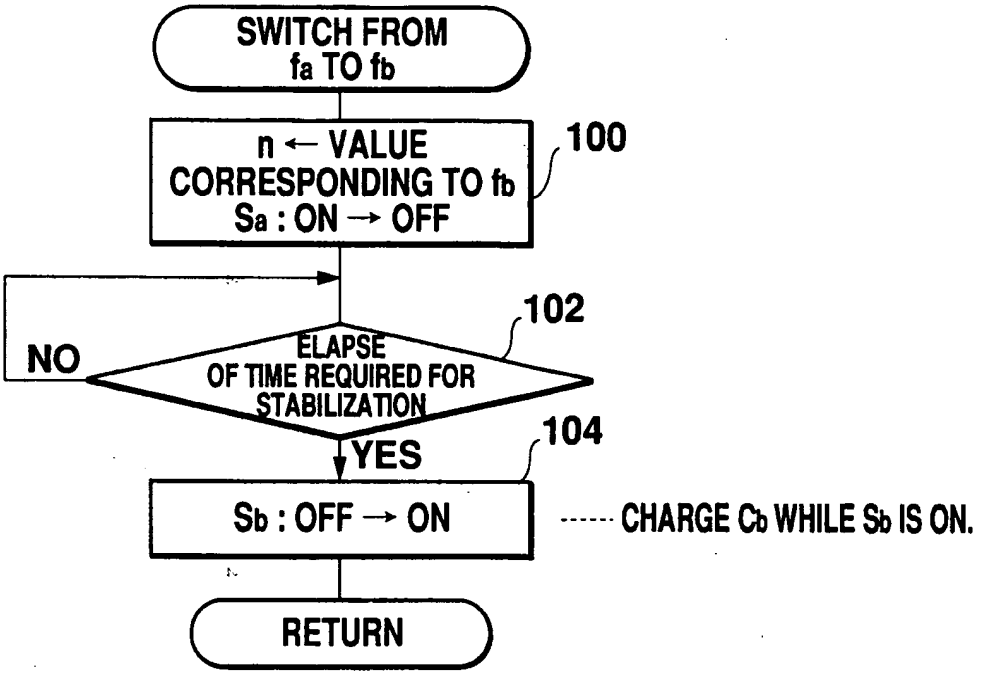
SWITCH FROM fa TO fb
n ← VALUE CORRESPONDING TO fb
Sa : ON → OFF
100
NO
ELAPSE OF TIME REQUIRED FOR STABILIZATION
102
YES
104
Sb : OFF → ON
------ CHARGE Cb WHILE Sb IS ON.
RETURN

Fig. 5

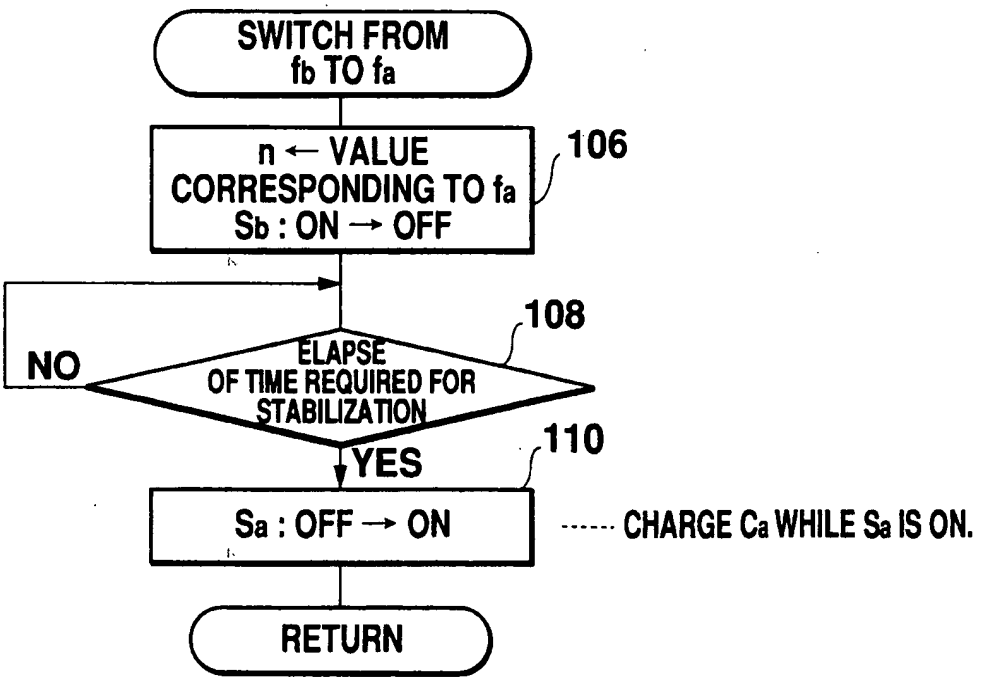
SWITCH FROM fb TO fa
n ← VALUE CORRESPONDING TO fa
Sb : ON → OFF
106
NO
ELAPSE OF TIME REQUIRED FOR STABILIZATION
108
YES
110
Sa : OFF → ON
------ CHARGE Ca WHILE Sa IS ON.
RETURN

Fig. 6

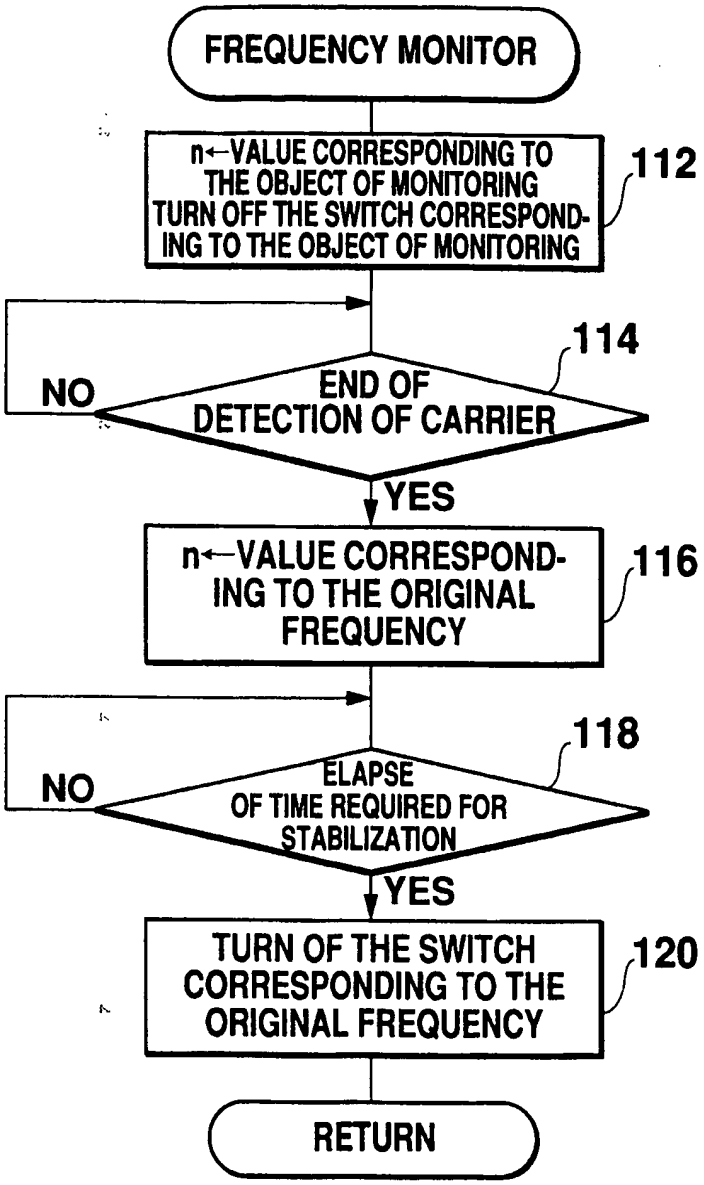
FREQUENCY MONITOR
n←VALUE CORRESPONDING TO THE OBJECT OF MONITORING TURN OFF THE SWITCH CORRESPONDING TO THE OBJECT OF MONITORING
112
114
NO
END OF DETECTION OF CARRIER
YES
n←VALUE CORRESPONDING TO THE ORIGINAL FREQUENCY
116
118
NO
ELAPSE OF TIME REQUIRED FOR STABILIZATION
YES
TURN OF THE SWITCH CORRESPONDING TO THE ORIGINAL FREQUENCY
120
RETURN

Fig. 7

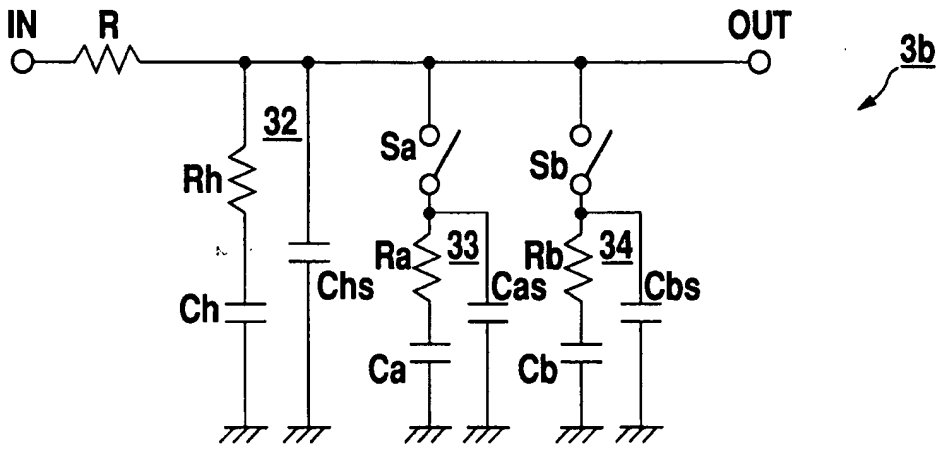

Fig. 8

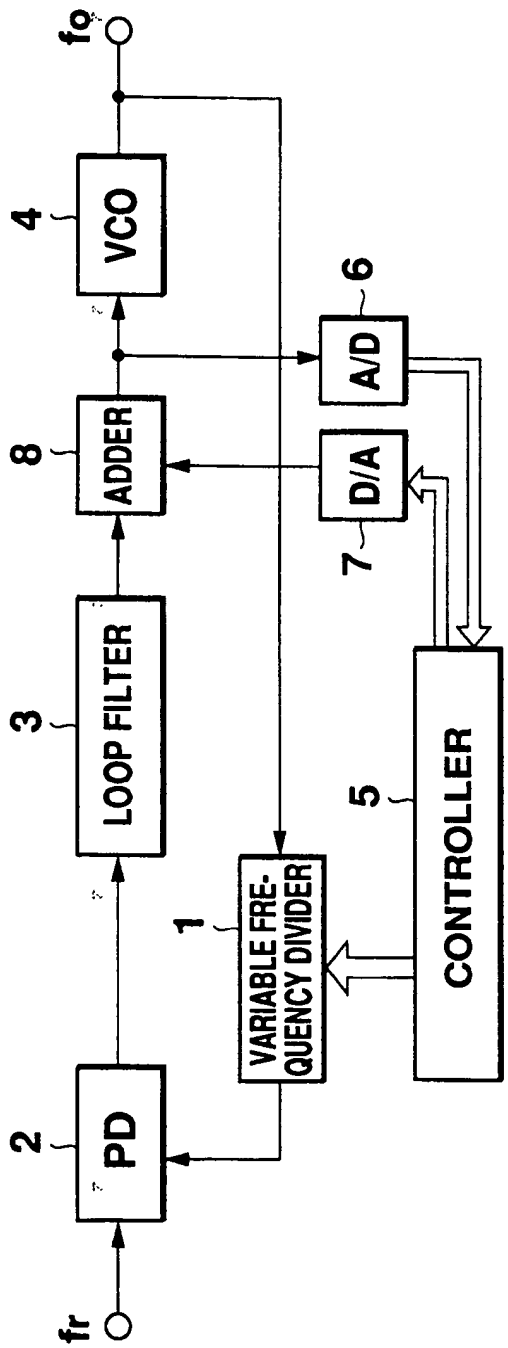
fo
4
VCO
6
A/D
8
ADDER
D/A
7
3
LOOP FILTER
5
CONTROLLER
1
VARIABLE FRE-
QUENCY DIVIDER
2
PD
fr

Fig. 9

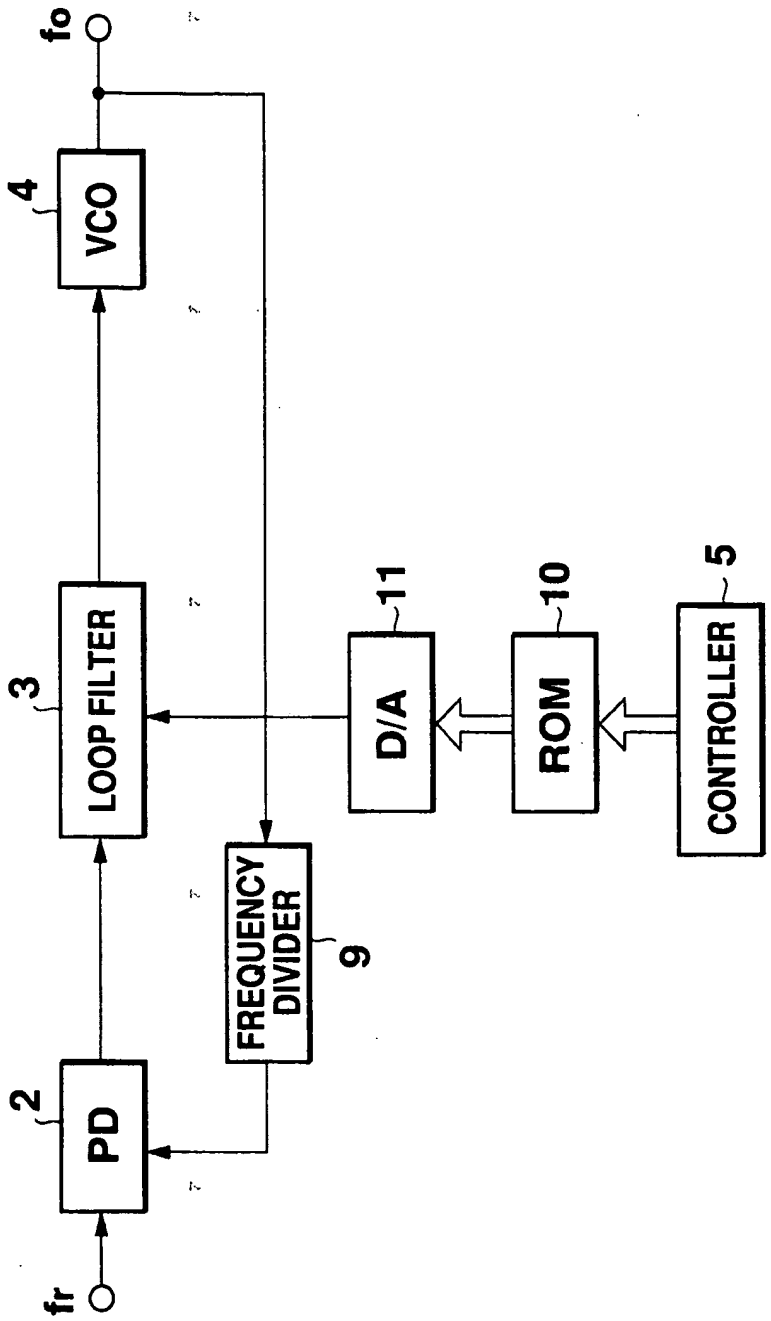
fo
4
VCO
3
LOOP FILTER
11
D/A
10
ROM
5
CONTROLLER
FREQUENCY DIVIDER
9
2
PD
fr

Fig. 10